CURRICULUM VITAE
MANAS BAJAJ

BIOSKETCH

Manas Bajaj is a Senior Research Engineer at InterCAX, LLC (www.InterCAX.com). He has been involved with InterCAX since its inception in 2003 and worked as a part-time researcher from 2005 till 2007. He is also a PhD candidate in Mechanical Engineering at Georgia Tech—expected completion in Spring 2008. He received his M.S. in Mechanical Engineering from Georgia Tech, and B.Tech. in Ocean Engineering and Naval Architecture from Indian Institute of Technology (IIT), Kharagpur, India.

His industrial and research experience spans over 7 years across several organizations—NIST, NASA, Rockwell Collins, IBM, Sandia, Lockheed Martin, and InterCAX in USA; and Hindustan Shipyard Limited and Mazagaon Dock Limited in India.

His research interests are in the realm of computer-aided design and engineering (CAD/CAE), next generation modeling and simulation methods, engineering frameworks, and open standards in the context of product and system lifecycle management. He has authored several publications, including those that won the Robert E. Fulton best paper award at ASME CIE 2005 and the session best paper award at Semicon West 2003. As a part of his PhD dissertation, Manas is developing the Knowledge Composition Methodology aimed at reducing the time and cost of creating simulation templates, thereby increasing the efficiency and extent of simulation-based design of engineering artifacts.

Manas has been the lead developer of *XaiTools Electronics*™ — a modeling and simulation toolkit for electronics artifacts originally developed at Georgia Tech (while he was a graduate researcher), and advanced and commercialized at InterCAX (while he was a part-time researcher) during NIST SBIR Phase 1 and Phase 2 periods. He is currently heading the R&D efforts on this toolkit at InterCAX during the NIST SBIR Phase 2 period. Manas has been actively involved in the development, implementation, and testing of the STEP AP210 standard. STEP AP210 is a core component of the innovative methods embodied in *XaiTools Electronics*™.

He serves as a technical team member at PDES Inc. representing Georgia Tech and InterCAX, is involved in the development and deployment of the OMG SysML specifications, and is an ASME member.

CONTACT INFORMATION

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ACADEMIC QUALIFICATIONS

- **Doctor of Philosophy (PhD)**, Mechanical Engineering, Georgia Institute of Technology, **(expected Spring 2008)**
  - Dissertation title: *A Knowledge Composition Methodology for Efficient Analysis Problem Formulation in Simulation-based Design*
  - Major: Computer-aided Engineering and Design; Minor: Industrial and Systems Engineering
  - GPA: 4.0/4.0 (Major and Minor)

- **Master of Science (MS)**, Mechanical Engineering, Georgia Institute of Technology, **2003**
  - Major: Computer-aided Engineering and Design
  - GPA: 4.0/4.0

- **Bachelor of Technology (BTech) Honours**, Ocean Engineering and Naval Architecture, Indian Institute of Technology (IIT), Kharagpur, India, **2001**
  - Thesis title: *An Integrated Shipbuilding Market Forecasting Method*
  - Department Rank: 1 of 18
  - GPA: 9.27/10

INDUSTRIAL EXPERIENCE

- **InterCAX LLC**, USA (www.intercax.com) – Full-time professional
  - Senior Research Engineer
  - Period: Dec 20, 2007 – present

- **InterCAX LLC**, USA (www.intercax.com) – Part-time co-op
  - Period: 2005–2007
  - Projects:
    - Thermo-mechanical warpage assessment of printed circuit assemblies / boards, developed a commercial tool (www.intercax.com/warpage)
    - Developing next-generation tools for simulation-based design, based on open standards-based product models

- **IBM Extreme Blue** internship program (www.ibm.com/extremeblue) – Internship
  - Period: May-Aug 2004
  - Project: Diagnostics for open standards-based product lifecycle management (PLM)

- **Rockwell Collins**, Cedar Rapids, Iowa, USA (www.rockwellcollins.com) – Full-time co-op
  - Period: May-Aug 2003
  - Project: Design-for-manufacturability analysis of electronics product families

- **Mazagon Dock Limited**, Mumbai, India (www.mdlindia.com) – Full-time internship
  - Period: May-July 2000
  - Projects: Passenger space allocation for a cruise ship, hydrostatic computations for a barge, and dry-docking principles for repairing damaged ships

- **Hindustan Shipyard Limited, Visakhapatnam, India** (http://hsl.nic.in/) – Short-term practical training
  - Period: Dec 1999
  - Project: Design and manufacturing processes in shipyards

RESEARCH & DEVELOPMENT EXPERIENCE

(Dec 2007 – present): Senior Research Engineer,
InterCAX LLC – www.InterCAX.com

(Aug 2001 – Dec 2007): Graduate Research Assistant, Engineering Information Systems Lab**,**
Georgia Institute of Technology – www.eislab.gatech.edu/people/manas

Research areas, summary, and associated projects

- **Area 1**: **Simulation-based design | Design-analysis integration and automation**

  - **Value**: Reduce time to analyze design alternatives, increase product quality, and enhance collaboration between designers and analysts

  - **Description**: The focus of this research area is to develop methods, models and tools for efficient creation of analysis models for evaluating design alternatives across multiple disciplines. The outcome of this research is the *Knowledge Composition Methodology (KCM)* that enables automated creation, reconfiguration and verification of analysis models that may be solved using multiple solution methods (such as analytical methods, finite element method (FEM)), and multiple solvers (such as ABAQUS, ANSYS) for each solution method. Specifically, the methodology shall enable the creation of analysis models for (a) design alternatives with variable *system topology* — characterized using number and type of components and interactions, and (b) different idealizations specified by analysts.

  - **Projects:**
    - (NIST and Georgia Tech): Design-Analysis Integration – www.eislab.gatech.edu/projects/nist-dai/
    - PhD research: *Knowledge Composition Methodology* – abstract at www.eislab.gatech.edu/people/manas/

- **Area 2: Thermo-mechanical analysis of electromechanical products | Design-for-manufacturability (DFM)**
  - **Value**: Reduce cost of non-conformance of electromechanical products, increase product quality
  - **Description**: This research area builds on the methods developed in Area 1 (above). Two primary thrusts in this area are: (a) capture DFM knowledge and automate DFM analyses during the design process, and (b) develop methods and tools for thermo-mechanical warpage (out-of-plane deformation) assessment of printed circuit boards (PCBs) and assemblies (PCAs) – **now available as a commercial tool** (see InterCAX bullet and web link below).
  - **Projects**:
    - (Rockwell Collins and Georgia Tech): Design-for-Manufacturability – www.eislab.gatech.edu/projects/rci-sfm/
    - (NIST and Georgia Tech): PCA/PCB Warpage – www.eislab.gatech.edu/projects/nist-warpage/
    - **Commercial tool for warpage assessment** (thrust b): www.intercax.com/warpage/
- **Area 3: Information modeling and knowledge representation methods and languages | Open standards**
  - **Value**: Represent, share, and reuse engineering knowledge to reduce time-to-market of products
  - **Description:** The objective of this research area is to represent the breadth and depth of engineering information and knowledge such that it may be reused across different lifecycle processes (such as design, analysis, manufacturing, operation). This is founded on using open standards that provide non-proprietary, cross-discipline constructs to model and reuse this knowledge. Some key languages on which I have founded my research are: STEP (ISO 10303) family of ontologies (www.tc184-sc4.org/), OMG SysML (www.omgsysml.org), and UML (www.uml.org) languages.
  - **Projects:**
    - (NIST and Georgia Tech): Warpage Analysis – www.eislab.gatech.edu/projects/nist-warpage/
    - (Sandia National Labs and Georgia Tech): Semantic Frameworks for Distributed Simulation
    - (NASA GSFC, NASA JPL, Lockheed Martin, and Georgia Tech): Composable Object Knowledge Representation – www.eislab.gatech.edu/projects/nasa-ngcobs/
- **Area 4: Product lifecycle management (PLM) | Open standards-based PLM frameworks**
  - **Value:** Develop software environments (frameworks) for automating PLM processes
  - **Description:** The focus of this research area is to (a) leverage open standards (Area 3 above) to develop a foundational model for representing product-related information (such as requirements, form, function, behavior, analysis) across different lifecycle phases, and (b) develop software environments (frameworks) to populate, view, relate, and use these diverse sets of information across different lifecycle processes. This also involves developing metrics for assessing the degree to which engineering information created using commercial-off-the-shelf (COTS) tools is compliant with open standards.
  - **Projects**
    - IBM Extreme Blue internship program: Recognizing the value of standards-based PLM – papers presented at 2005 ASME International DETC/CIE – www.eislab.gatech.edu/people/manas
    - (NASA JPL and Georgia Tech): Advanced Collaborative Engineering Environments – www.eislab.gatech.edu/projects/nasa-jpl-cee/

Tools[1]

I am actively involved in developing algorithms and software tools as test beds for concepts and methodologies developed during research. Some of these tools are:

- **Production Tools** (including early R&D prototypes)
  - *XaiTools PWA-B*^{TM} for thermo-mechanical warpage analysis and stackup design of printed circuit boards (being incorporated into *XaiTools Electronics*^{TM})

[1] Additional information available upon request

- *XaiTools Electronics™* for modeling and simulation of electronics artifacts — currently incorporates *XaiTools PWA-B™* for warpage analysis of PCBs and PCAs; work-in-progress to incorporate *XaiTools Chip Package™* for thermal and thermo-mechanical analyses of chip packages
- *SFM DFM Framework* — a rule-based expert system for design-for-manufacturability evaluation of electronics products

- **Research Prototypes**
  - *Semantic Technology plugin for Protégé ontology editor* for automated creation of ontologies for distributed federated simulations

TEACHING EXPERIENCE

- **Teaching Associate, Georgia Institute of Technology**
  - Period: Spring 2005
  - Course: *Modeling and Simulation in Design* (*ME8813*) - graduate level (MS/PhD) course

- **Teaching Assistant, Georgia Institute of Technology**
  - Period: Fall 2002
  - Course: *Engineering Graphics and Visualization (ME 1770)* - undergraduate level course

AWARDS AND ACHIEVEMENTS

- **Robert E. Fulton Best Paper Award**, Engineering Information Management Track, ASME International DETC/CIE 2005, Long Beach, CA, USA
- **Best Paper Award**, Session 210, IEMT Semicon West 2003 conference, San Jose, CA, USA
- Elected for ***Who's Who Among Students in American Colleges and Universities***, 2005 and 2006
- **Best Project Award, 2001**, Department of Ocean Engineering & Naval Architecture, Indian Institute of Technology, Kharagpur, India
- **President's Silver Medal** for 1st ranked undergraduate student (of 18 students), 1997-2001, Department of Ocean Engineering and Naval Architecture, Indian Institute of Technology, Kharagpur, India
- **Dr. J.C. Ghosh Memorial Award** for the most outstanding student, 2001, Department of Ocean Engineering & Naval Architecture, Indian Institute of Technology, Kharagpur, India.
- **Lloyds Register of Shipping (UK) Scholarship** for the 1st ranked undergraduate student (of 18 students), 2000-2001, Department of Ocean Engineering & Naval Architecture, Indian Institute of Technology, Kharagpur, India.
- **The J.N. Tata Endowment Award** for graduate studies, 2001, Mumbai, India.
- **Honorary Mention by The Director,** Indian Institute of Technology, Kharagpur, India for scoring semester GPA of 10.0 /10.0 in Fall 2000.
- Cumulative GPA 9.27/10.0 (undergraduate) - highest in the last decade (1991-2001), Department of Ocean Engineering & Naval Architecture, Indian Institute of Technology, Kharagpur, India.

PUBLICATIONS[2]

- **Bajaj, M**., Peak, R.S. and Paredis, C.J.J. (2007). *Knowledge Composition for Efficient Analysis Problem Formulation, Part 1: Motivation and Requirements*. ASME International Design Engineering Technical Conferences & Computers and Information in Engineering Conference, Las Vegas, NV, USA September 4-7, 2007.

- **Bajaj, M**., Peak, R.S. and Paredis, C.J.J. (2007). *Knowledge Composition for Efficient Analysis Problem Formulation, Part 2: Approach and Analysis Meta-Model*. ASME International Design Engineering Technical Conferences & Computers and Information in Engineering Conference, Las Vegas, NV, USA September 4-7, 2007.

- Peak, R.S., Burkhart, R., Friedenthal, S., Wilson, M.W., **Bajaj, M**. and Kim, I. (2007). *Simulation-Based Design Using SysML, Part 1: A Parametrics Primer*. INCOSE International Symposium, San Diego, CA, USA June 24-28, 2007.

- Peak, R.S., Burkhart, R., Friedenthal, S., Wilson, M.W., **Bajaj, M.** and Kim, I. (2007). *Simulation-Based Design Using SysML, Part 2: Celebrating Diversity by Example*. INCOSE International Symposium, San Diego, CA, USA June 24-28, 2007.

[2] Listed in a chronological order

- **Bajaj, M.**, Peak, R., Zwemer, D., Thurman, T., Klein, L., Liutkus, G., Brady, K., Messina, J. and Dickerson, M. (2006). *Automating Thermo-Mechanical Warpage Estimation of PCBs/PCAs Using a Design-Analysis Integration Framework*. Mentor U2U, San Jose, CA, USA May 3-5, 2006.

- Klein, L., Peak, R., Thurman, T., Smith, G., Waterbury, S. and **Bajaj, M.** (2006). *Standards-based Environment for Electro-Mechanical Product Realization*. Mentor U2U, San Jose, CA, USA May 3-5, 2006.

- **Bajaj, M.**, Paredis, C., Rathnam, T. and Peak, R. (2005). *Federated Product Models for Enabling Simulation-based PLM*. ASME International Mechanical Engineering Congress and Exposition (IMECE), Orlando, FL, USA Nov 5-11, 2005.

- **Bajaj, M.**, Kim, I., Mocko, G., Peak, R., Udoyen, N., Wilson, M., Greene, D., Raines, B. and Srinivasan, V. (2005). *Diagnosing Engineering Information Interoperability, Recognizing the value of standards-based PLM – Part 1*. ASME DETC / CIE, Long Beach, CA, USA September 24-28, 2005.

- Kim, I., **Bajaj, M.**, Udoyen, N., Mocko, G., Peak, R. and Wilson, M. (2005). *Metrics for Degree-of-Openness of Engineering Information, Recognizing the value of standards-based PLM - Part 2,* ***Recipient of the Robert E. Fulton Best Paper Award***. ASME DETC/CIE, Long Beach, CA, USA September 24-28, 2005.

- **Bajaj, M.**, Peak, R., Klein, L., Dickerson, M. and Zwemer, D. (2005). *Standards-based Engineering Frameworks for Next-Generation PLM*. PLM World, Dallas, TX, USA May 2-6, 2005.

- **Bajaj, M.**, Peak, R., Zwemer, D., Thurman, T., Dickerson, M., Brady, K. and Messina, J. (2005). *Next Generation Simulation-based Design Technologies for Electronics Product Realization*. The 7th NASA-ESA Workshop on Product Data Exchange (PDE), MARC, Georgia Tech, Atlanta, GA, USA April 19-22, 2005.

- **Bajaj, M.**, Paredis, C., Rathnam, T. and Peak, R. (2005). *Federated Product Models for Simulation-based PLM*. The 7th NASA-ESA Workshop on Product Data Exchange (PDE), MARC, Georgia Tech, Atlanta, USA April 19-22, 2005.

- Peak, R., Friedenthal, S., Moore, A., Burkhart, R., Waterbury, S., **Bajaj, M.** and Kim, I. (2005). *Experiences Using SysML Parametrics to Represent Constrained Object-based Analysis Templates*. 7th NASA-ESA Workshop on Product Data Exchange (PDE), Atlanta, GA, USA May 2-6, 2005.

- Zwemer, D., **Bajaj, M.**, Peak, R., Klein, L. and Dickerson, M. (2005). *Standards-based Engineering Frameworks for Next-Generation PLM*. The 7th NASA-ESA Workshop on Product Data Exchange (PDE), Atlanta, GA, USA April 19-22, 2005.

- Zwemer, D., Bajaj, M., Peak, R., Thurman, T., Brady, K., McCarron, S., Spradling, A., Dickerson, M., Klein, L., Liutkus, G. and Messina, J. (2004). *PWB Warpage Analysis and Verification Using an AP210 Standards-based Engineering Framework and Shadow Moiré*. IEEE EuroSimE, Brussels, Belgium May 10-12, 2004.

- **Bajaj, M.**, Peak, R., Wilson, M., Kim, I., Thurman, T., Benda, M., M.C.Jothishankar, Ferreira, P.M. and Stori, J. (2003). *Towards Next-Generation Design-for-Manufacturability (DFM) Frameworks for Electronics Product Realization,* ***Recipient of the Best Paper Award for Session 210***. IEMT Semicon West, San Jose, CA, USA July 16-18, 2003.

- **Bajaj, M.**, Peak, R. and Fulton, R.E. (2003). *Customizing Next-Generation Multidisciplinary Product Realization Frameworks*. ASME International DETC/CIE, Chicago, IL Sep 2-6, 2003.

- Peak, R., **Bajaj, M.**, Wilson, M., Kim, I., Thurman, T., M.C.Jothishankar, Ferreira, P., Stori, J., Mukhopadhyay, D., Tang, D., Liutkus, G. and Klein, L. (2003) *Enhancing Design-for-Manufacturability Using the ISO 10303 Standard for Electronics Design: AP210*. Aerospace Product Data Exchange (APDE) Workshop, NIST, Gaithersburg, MD, USA April 7-10, 2003.

- Matsuki, R., Peak, R., Zeng, S., Wilson, M., Kim, I. and **Bajaj, M.** (2002). *Design-Analysis (Thermal and Mechanical) Integration Research for Electronic Packaging*. Semicon Japan 2002, Japan.

- Peak, R., Wilson, M., Kim, I., Udoyen, N., **Bajaj, M.**, Mocko, G., Liutkus, G., Klein, L. and Dickerson, M. (2002). *Creating Gap-Filling Applications Using STEP Express, XML, and SVG-based Smart Figures - An Avionics Example*.

NASA-ESA Workshop on Aerospace Product Data Exchange, ESA/ESTEC, Noordwijk (ZH), The Netherlands April 9-12, 2002.

REPORTS & WHITEPAPERS

- Peak, R. and **Bajaj, M**. (2007). *Capturing Design Process Information and Rationale to Support Knowledge-Based Design and Analysis Integration,* NIST-Georgia Tech Design-Analysis Integration Project (Phase 3). Atlanta, GA, USA, Georgia Tech.

- Peak, R., **Bajaj, M.**, Kim, I. and Mocko, G. (2006). *Capturing Design Process Information and Rationale to Support Knowledge-Based Design and Analysis Integration,* NIST-Georgia Tech Design-Analysis Integration Project (Phase 2). Atlanta, GA, USA, Georgia Tech.

- Peak, R., Mocko, G., **Bajaj, M.** and Kim, I. (2004). *Capturing Design Process Information and Rationale to Support Knowledge-Based Design and Analysis Integration,* NIST-Georgia Tech Design-Analysis Integration Project (Phase 1). Atlanta, GA, USA, Georgia Tech.

- **Bajaj, M.**, Mocko, G., Kim, I., Udoyen, N., Wilson, M., Peak, R., Paredis, C., Greene, D., Srinivasan, V. and Raines, B. (2004). *GT-Diagnostics: Recognizing the value of standards-based PLM systems*. Atlanta, GA, USA, Georgia Tech and IBM.

PROFESSIONAL AFFILIATIONS

- Technical team member, PDES, Inc. (international consortium for development of ISO STEP standards) – http://pdesinc.aticorp.org/
- Technical member, Georgia Tech team for contributions to OMG SysML standard
- Student Member, American Society of Mechanical Engineers (ASME)

COMPUTING SKILLS & EXPERIENCE

Modeling languages:	EXPRESS (IS0 10303-11), UML, SysML, XML
Programming languages:	Java, Python, C/C++, SQL
Programming toolkits:	LKSoft JSDAI (STEP) and AP210 toolkit, Batik (SVG), JUnit (testing)
Open standard ontologies:	ISO STEP standards
Open standard-based apps:	IDA-STEP (ISO STEP); MagicDraw, ARTiSAN Studio, EmbeddedPlus (UML / SysML)
Markup languages:	XML, HTML, SVG
Expert system languages:	CLIPS, JESS, Kappa
CAD applications:	Pro/E, Catia, UGS NX, AutoCAD, Solid Edge, EAGLE
CAE applications:	ANSYS, ABAQUS, Simmetrix suite of FE pre-processing tools
Other tools :	iSIGHT (optimization), MATLAB (computation)
IDE tools:	Eclipse, CVS, Bugzilla

REFERENCES

Available upon request