**Proceedings of InterPACK'01**
The Pacific Rim/ASME International Electronic Packaging
Technical Conference and Exhibition
**July 8–13, 2001, Kauai, Hawaii, USA**

**IPACK2001-15810**

# AN OBJECT-ORIENTED INTERNET-BASED FRAMEWORK FOR CHIP PACKAGE THERMAL AND STRESS SIMULATION

**[1]Russell S. Peak, [2]Ryuichi Matsuki, [1]Miyako W. Wilson, [1]Donald Koo,**
**[1]Andrew J. Scholand, [2]Yukari Hatcho, [1]Sai Zeng**

[1]Engineering Information Systems Lab
Georgia Institute of Technology
Atlanta, Georgia USA
*http://eislab.gatech.edu/*

[2]Package Design Center
Shinko Electric Industries Co., Ltd.
Nagano, Japan
*http://www.shinko.co.jp/*

## ABSTRACT

Simulating the behavior of electronic chip packages like ball grid arrays (BGAs) is important to guide and verify their designs. Thermal resistance, thermomechanical stress, and electromagnetics impose some of the main challenges that package designers need to address. Yet because packages are composed of numerous materials and complex shapes, with current methods an analyst may spend hours to days creating simulations like finite element analysis (FEA) models.

This paper overviews work to reduce design cycle time by automating key aspects of FEA modeling and results documentation. The main objective has been automating FEA-based thermal resistance model creation for a variety of package styles: quad flat packs (QFPs), plastic BGAs (PBGAs), and enhanced BGAs (EBGAs). Pilot production tools embody analysis integration techniques that leverage rich product models and idealize them into FEA models. We have also demonstrated how the same rich product models can drive basic stress models with different idealizations.

In this framework, Internet standards like CORBA enable worldwide access to simulation solvers (e.g., Ansys and Mathematica). Automation and ease-of-use enable access by chip package designers and others who are not simulation specialists. Pilot industrial usage has shown that total simulation cycle time can be decreased 75%, while modeling time itself can be reduced 10:1 or more (from hours to minutes).

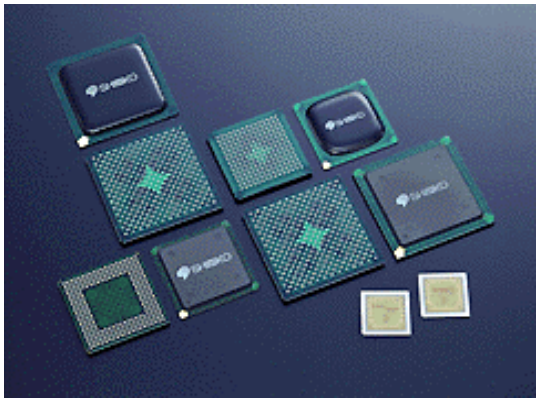


Figure 1 - Chip packages: plastic ball grid arrays (PBGAs)

## KEY WORDS

chip package, ball grid array (BGA), quad flat packs (QFP), thermal resistance, analysis integration, variable topology multi-body (VTMB), constrained objects (COBs), multi-representation architecture (MRA), CORBA, Internet inter-object request broker protocol (IIOP), Ansys, Mathematica, *XaiTools ChipPackage*™

## NOMENCLATURE

| | |
|---|---|
| APM | analyzable product model |
| BGA | ball grid array |
| COB | constrained object |
| CORBA | common object request broker architecture |
| EBGA | enhanced BGA |
| MRA | multi-representation architecture |
| PBGA | plastic BGA |
| QFP | quad flat pack |
| STEP AP210 | STEP standard for electronic products |
| VTMB | variable topology multi-body |
| XAI | X-analysis integration (X= design, mfg., etc.) |
| XCP | *XaiTools ChipPackage*™ |
| XFW | *XaiTools FrameWork*™ |

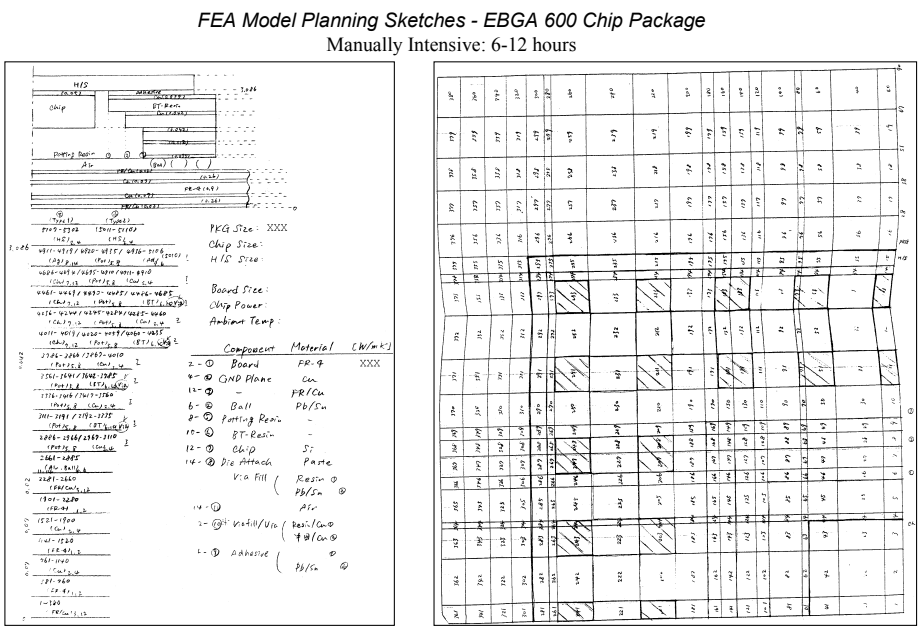



Figure 2 - Traditional creation of variable topology multi-body (VTMB) FEA models

## 1. INTRODUCTION

During the design of chip packages like quad flat packs (QFPs) and ball grid arrays (BGAs) (Figure 1), it is necessary to ensure they perform acceptably regarding criteria like thermal resistance, thermomechanical reliability, and electromagnetic behavior. While CAD and CAE tools have continued to advance, chip package complexity has also increased, making checking such criteria by physical behavior simulation a challenging proposition.

For example, it can take an experienced analyst 6-12 hours to develop the finite element model for the thermal resistance analysis of a QFP or BGA[1]. Figure 2 illustrates how the complexity of such models is caused by factors including the following:

1) Various considerations necessitate the use of idealized geometry in such simulations (e.g., mesh complexity, solution time, lack of details in early design stages, and better simulation).[2]
2) Even so, accurate chip package analysis models must consist of a number of idealized bodies (e.g., 20-30 bodies) of different idealized materials (e.g., 10 or so). The finite element method requires that nodes match between these bodies.
3) These bodies are tightly packed together. Thus the meshing of one body can strongly impact the meshing of bodies that are not directly adjacent to it. We use the term coupled **variable topology multi-body** (VTMB) model (Koo 2000) to describe this type of problem (Figure 3). Typically labor-intensive "chopping" is required to transform the analytical model into an FEA geometry model that can then be properly meshed.
4) The idealized bodies may not be part of patterns that are regularly repeated *en masse*.
5) The geometric idealizations that are significant for simulating one type of behavior may not be the same as those for another (e.g., stress vs. temperature).

This paper overviews work in Phase 1 of a collaborative effort between Shinko and Georgia Tech. It describes how engineering information technology has been combined with traditional CAE techniques to address the above issues.

## 2. APPROACH

The multi-representation architecture (MRA) for CAD-CAE interoperability and associated ubiquitization methodology (Peak, Fulton et al. 1998; Peak 1999; Peak, Scholand et al.

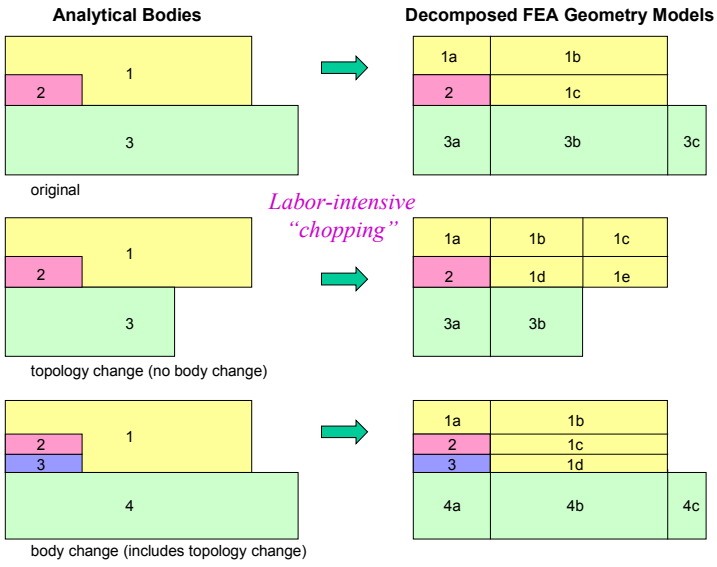



Figure 3 - Characteristics of VTMB FEA models

[1] Based on Shinko estimates for typical practice.

[2] Gordon (Gordon 2001) underscores the general difference between idealized analysis geometry vs. design geometry as typically required for two classes of analysis termed Categories II and III. Category II (CAD-centric) takes detailed design geometry and idealizes it for analysis. Category III (CAE-centric) takes analysis geometry and results and uses them as starting points to synthesize detailed design geometry. He defines Category I as the case where the two geometries are the same, which typically is feasible in cases of a distinct single material part. Today's CAD and CAE tools handle Category I well, leading many to believe that CAD-CAE interoperability is a solved problem. But Gordon and others show how Categories II and III continue to pose interoperability challenges, as idealization/synthesis transformations in these categories are largely manually driven today.

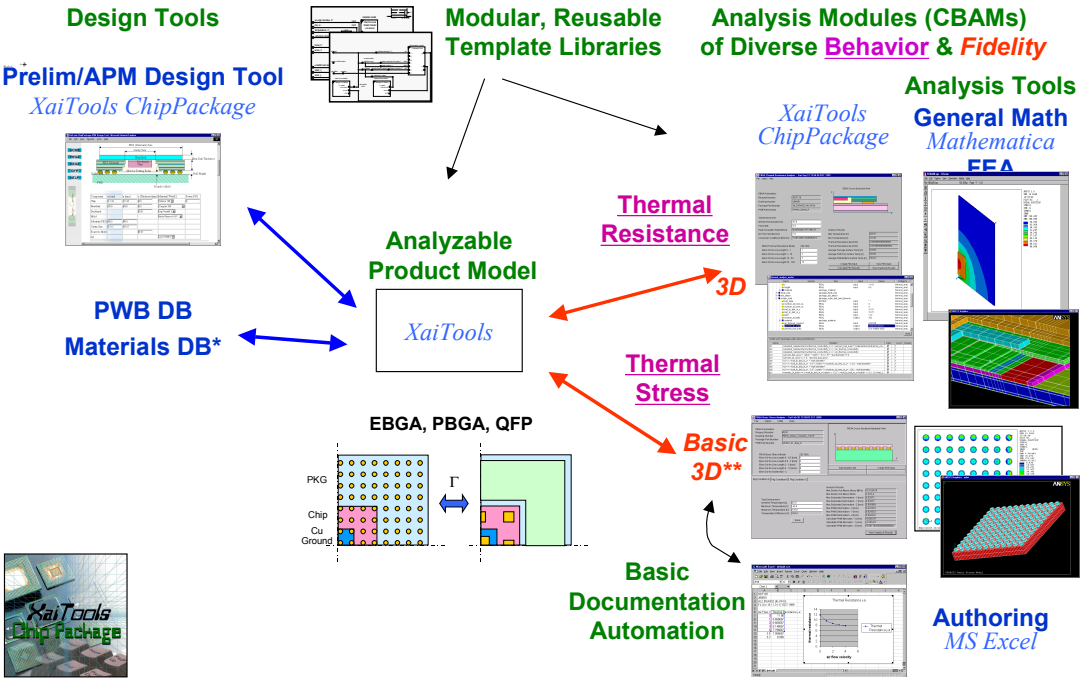



Figure 4 - Interoperability framework for chip package design & analysis (Phase 1 panorama)

1999; Peak, Scholand et al. 1999; Peak 2001) were applied and extended in Phase 1 to provide automated chip package analysis capabilities. Figure 4 is a panorama of this work, which shows the connection between CAD tools (on the left) with general purpose CAE tools (on the right) via reusable, modular template libraries. Other efforts have applied the MRA concepts and produced similar high diversity panoramas for airframe structural analysis and circuit board thermomechanical analysis.

The ubiquitization methodology begins by identifying what types of analysis are typically needed for a given family of products. For example, thermal resistance analysis is important for chip packages. In this work, Shinko already had in-house analysis procedures for reliably predicting thermal resistance. These procedures identified the proper types of boundary conditions and geometric idealizations to use. Phase 1 focused on automating analysis procedures for these package styles: quad flat packs (QFPs), plastic BGAs (PBGAs), and enhanced BGAs (EBGAs). The emphasis was on thermal resistance, but basic thermal stress was also addressed in the case of PBGAs.

Even with such procedures in place, typical practice today necessitates that an analyst apply them for each new design (Figure 2) by manually creating models in an appropriate CAE tool. Gordon and others note that for Category II problems, it is often easier to re-create analysis geometry in such tools than to use the actual detailed design geometry as a transformation input (see Footnote 2). Chip package thermal and stress analyses have different geometry for design vs. analysis and hence are best classified as Category II/III problems.

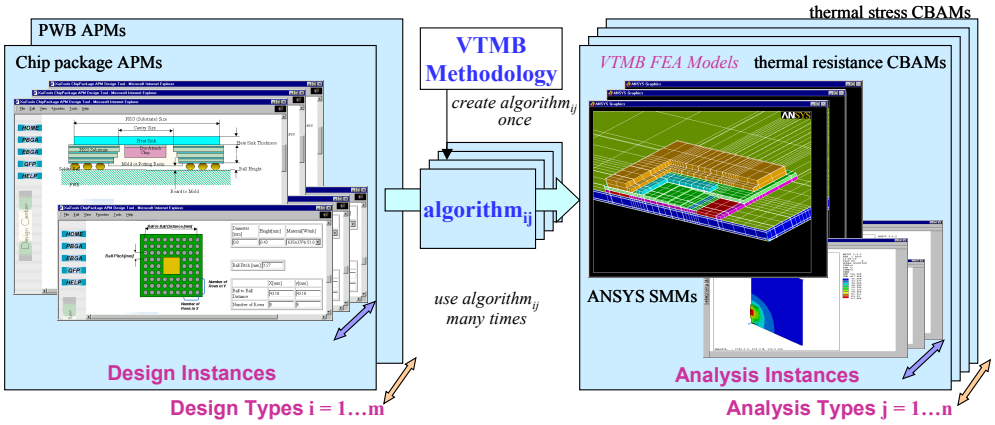



Figure 5 - Product information-driven VTMB FEA methodology (Koo 2000)

Given a mature analysis procedure like Shinko has, the ubiquitization methodology applies object-oriented thinking to divide the analysis procedure knowledge among the various concepts in the MRA (Figure 6). This modularization then aids implementation and analysis understanding. In this effort, Koo (Koo 2000) developed an MRA-based methodology for creating

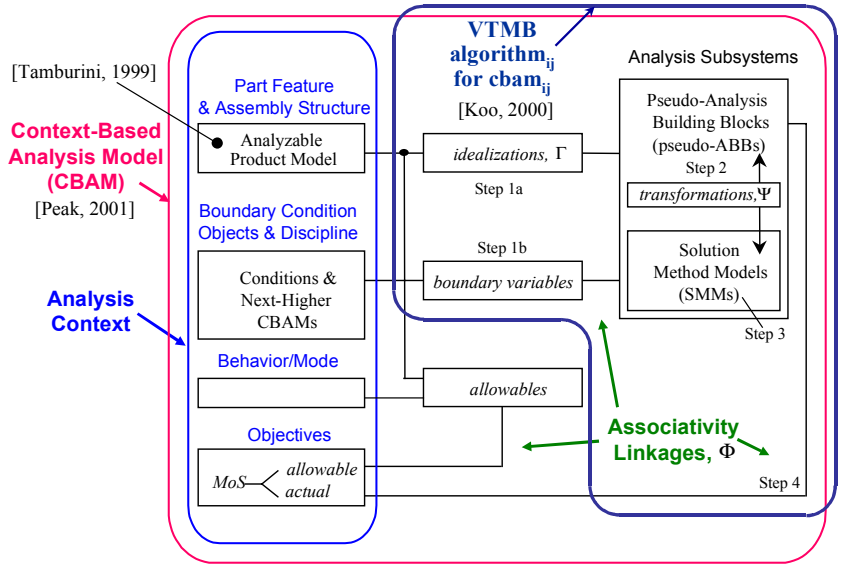



Figure 6 - Multi-representation architecture (MRA) for CAD-CAE integration (with VTMB extensions per (Koo 2000) )

algorithms (Figure 5) that handle the VTMB situations inherent in cases like chip package analysis.

## 3. USAGE OVERVIEW

The above concepts were implemented in specific tools as overviewed in Figure 4. *XaiTools ChipPackage* (XCP), developed at Georgia Tech, is the primary new tool. XCP is built upon *XaiTools FrameWork* (XFW), a reference implementation of the product-independent MRA concepts. XFW uses objects, constraints, and web computing to capture analysis intent and enhance interoperability among traditional CAD tools and general-purpose CAE tools (XFW 2001). This section walks through an XCP user scenario and highlights what happens underneath to achieve highly automated results.

1) A user creates a package design in XCP via a web-based user interface (Figure 7). Underneath an object-oriented package design model is created that includes geometric features and material models.
2) The user selects an analysis module (e.g., for thermal resistance analysis) which then processes the design model to calculate idealized parameters. Figure 8 is the user interface for an EBGA thermal resistance analysis module, which also shows a cross-section of the idealized 3D analysis model bodies.

XFW captures knowledge in constrained objects (COBs) (Wilson 2000) which can be browsed as shown in this figure. The attributes and sub-attributes of the resulting COB-based analyzable product model (APM) objects are shown in product-specific terms (e.g., `chip.height` and `die_attach`). Relations (constraints) among attributes are also included. Computable idealization relations like those in Figure 9 are thus stored with the objects that they apply to.

Underneath, XFW algorithms process COBs and transform their relations for solution by a general math tool (*Mathematica* in this case). XFW uses a CORBA[3] middleware architecture for highly automated interaction with such solvers, which may be located literally around the world (Figure 11).

3) Next the user enters boundary conditions (or uses default values for several standard air flow velocities) and clicks the button to initiate the FEA solution process (Figure 10).

Behind the scenes XCP applies the VTMB algorithm associated with this analysis module. This algorithm creates FEA tool commands (typically several hundred) based on the APM objects. Again XCP uses CORBA to send the inputs to a solver server, execute the FEA tool (*Ansys* in this case), and retrieve key results and graphics. The analysis module places these generic FEA results back into their product-specific context. It also performs other calculations on them if necessary (e.g., determining thermal resistances

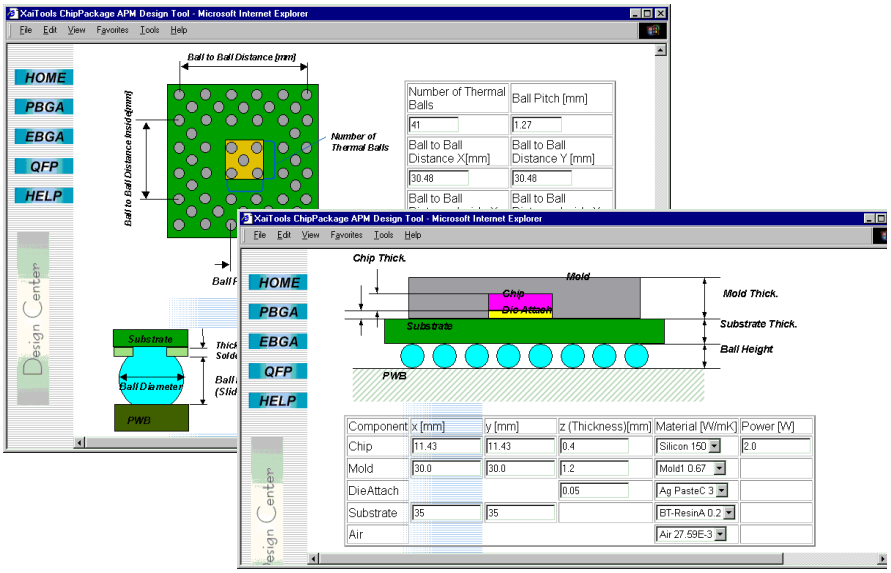



Figure 7 - Web-based chip package preliminary design tool (PBGAs)

[3] CORBA is a middleware standard to enable inter-object communication across diverse platforms and applications. See www.omg.org for further information.

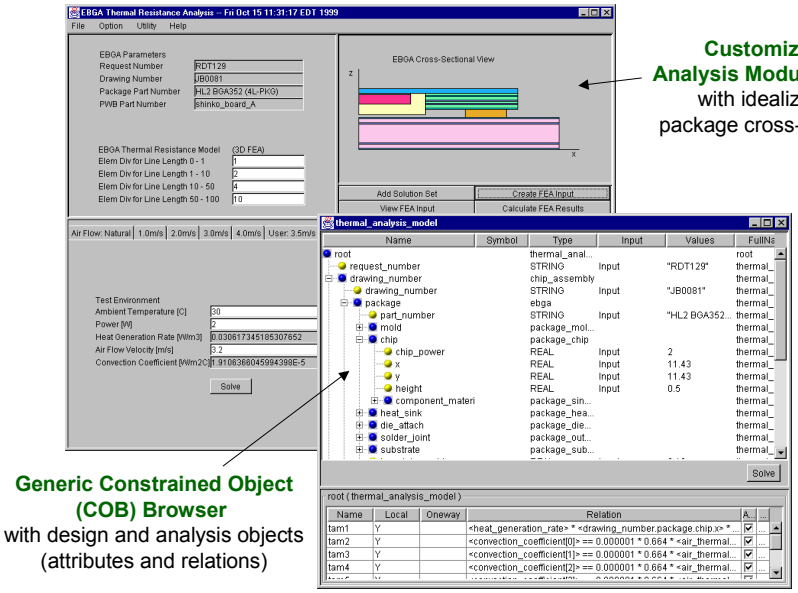



Figure 8 - Analysis module tool with product model inputs

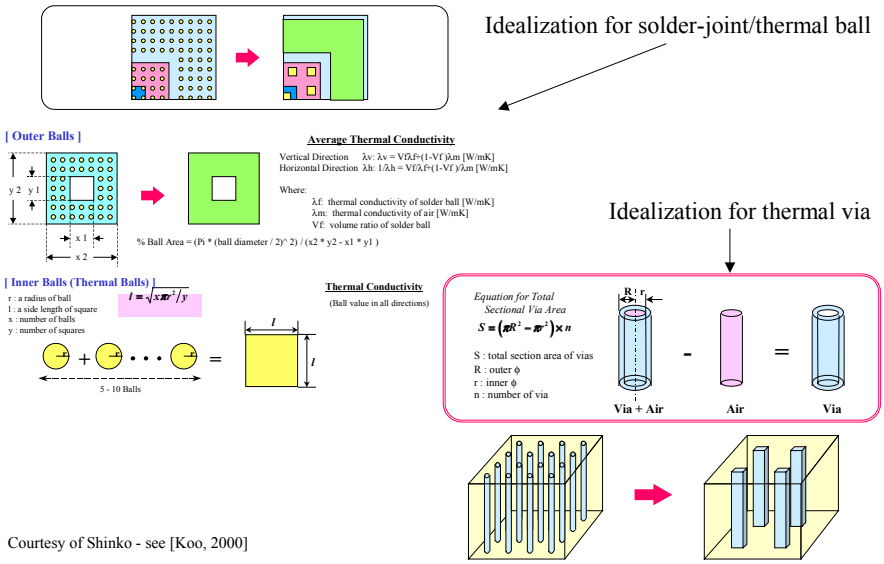



Figure 9 - Example chip package geometric idealizations
(for PBGA thermal analysis)

based on average package surface temperature and other values from the FEA results).

4) The user can then review graphical and numeric results for each air flow velocity and export summaries to MS Excel (lower portion of Figure 10) to aid in creating analysis reports.

## 4. EXAMPLE RESULTS

Figure 12 shows results for several modeling schemes where it is seen how thermal resistance decreases with increasing air flow velocity. This figure also shows that results from XFW (labeled Ansys, due to the solver it used) compare well with those from the traditional analyst-created method (labeled Cosmos) and with measured results.

Figure 13 gives a glimpse of FEA mesh model complexity for a PBGA case and a QFP case. These auto-generated models include a combination of small features, numerous tightly coupled bodies, and few step-and-repeatable patterns. Figure 14 illustrates some of the topological variations the VTMB-based algorithms in XCP can handle for these package families. For example, PBGAs can be modeled with and without thermal balls and vias, EBGAs can have variable numbers of steps and layers, and QFPs can have different lead connection methods. Referring back to Figure 2, one can imagine the negative impact of such changes for the analyst using the traditional method.

Figure 15 illustrates the impact of a relatively small design change on the FEA model. On the left hand side the heat spreader is thin and large (reaching almost to the edge of the package), whereas the design variation on the right has it as thick and smaller. Due to the relative thinness of bodies in idealized chip packages, each body may consist of only a few layers of elements in its z-direction. Thus they have strong coupling to each other with respect to FEA meshing, and resizing of features like the heat spreader can effect all layers. This is indeed the case here where the edge of the heat spreader necessitates creating mesh divisions in all the bodies below it. As the edge changes between the two cases shown, it changes the mesh topology of different bodies. Such changes cause re-numbering of nodes and elements, and thus would cause a great deal of re-work for the analyst using a method like that in Figure 2. The VTMB algorithms now handle such variations automatically.

Based on industrial usage and testing, Table 1 summarizes the analyst effort required for analysis model creation activities for various package types. Pilot usage of XCP and initial production usage indicate that FEA modeling time is reduced over 10:1 (from days/hours to minutes) and that overall simulation cycle time is reduced by more than 75%[4].

[4] Estimates are based on typical practice and test case experiences by Shinko Electric and Georgia Tech (recorded in Koo, 2000), and from Shinko evaluation in production usage (dated October, 2000). Durations in Table 1 are for model creation and do not include FEA solution time. Solution time ranges from 10 minutes (for some QFPs) to over 2 hours (for some PBGAs) on a Sun Ultra 10 workstation.

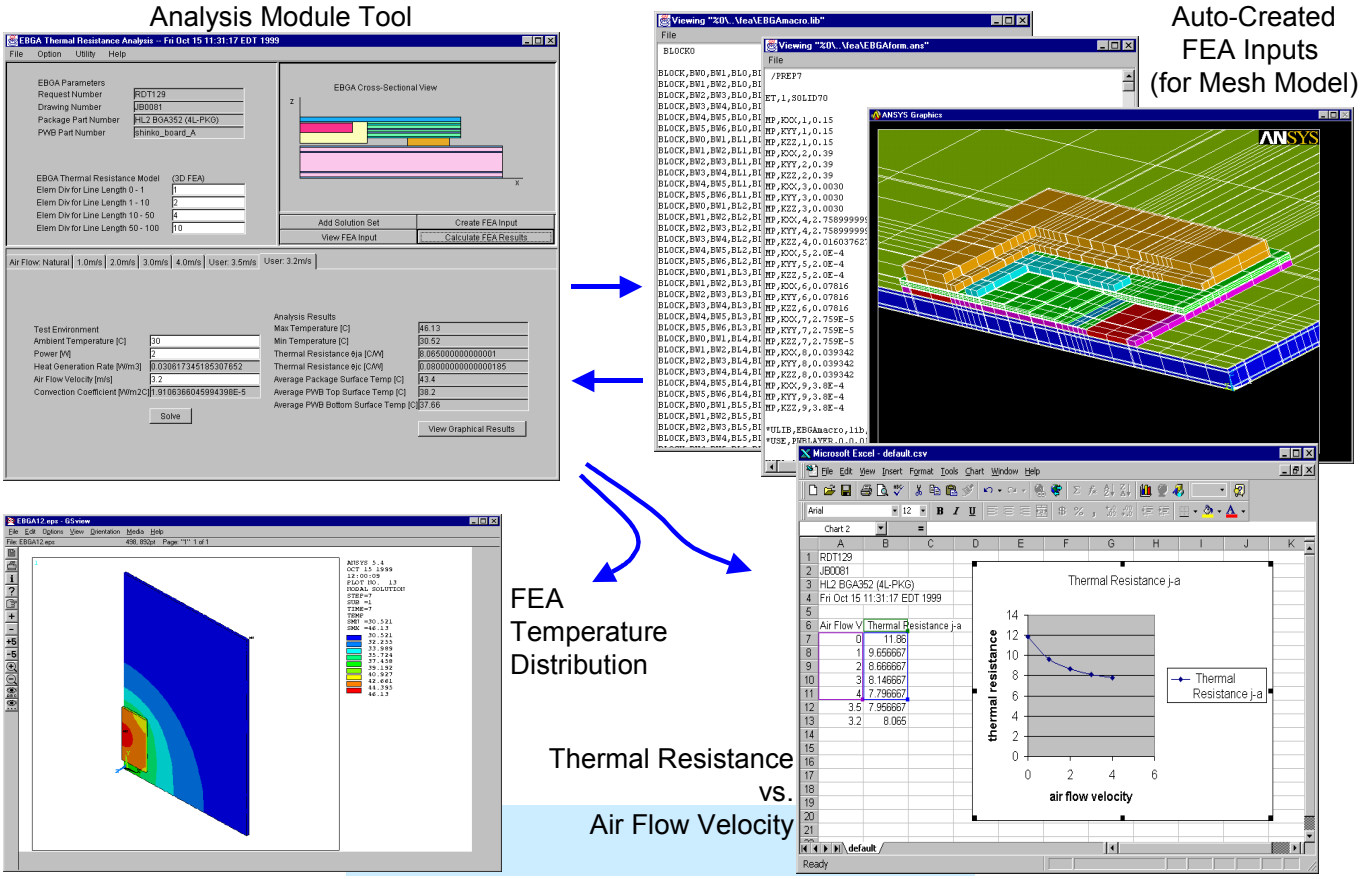



Figure 10 - Flow diagram for highly automated analysis

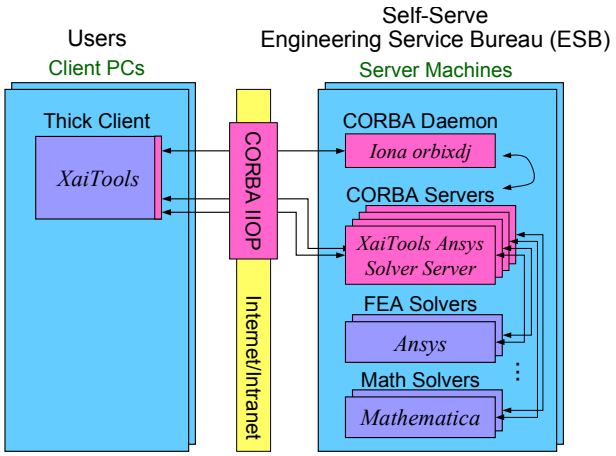
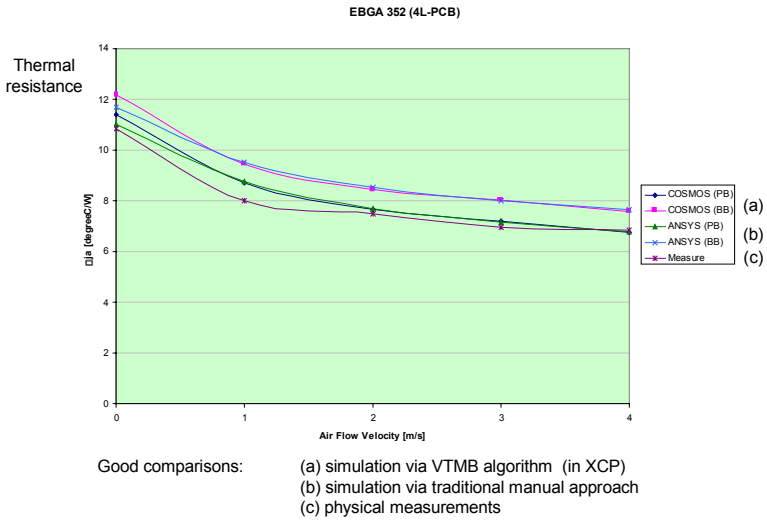
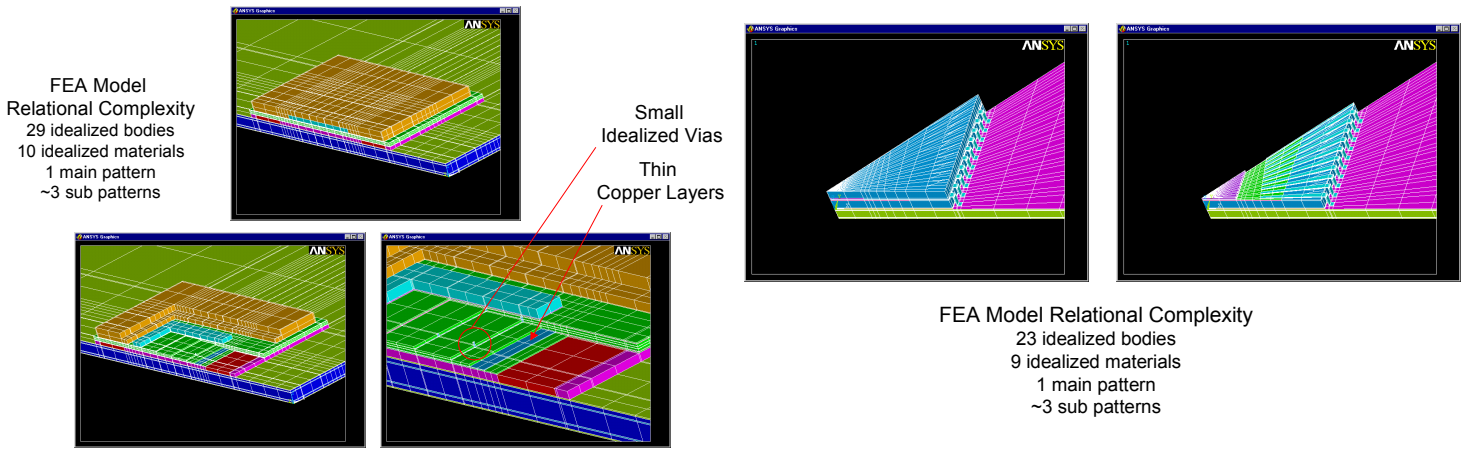



Figure 11 - Using Internet/Intranet-based analysis solvers (thick client architecture)




Good comparisons: (a) simulation via VTMB algorithm (in XCP)
(b) simulation via traditional manual approach
(c) physical measurements

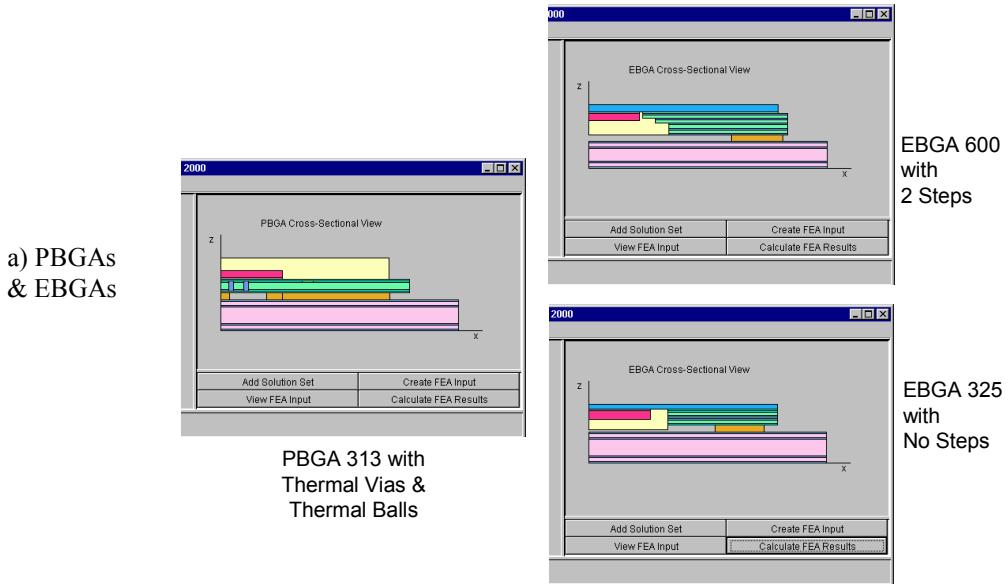
Figure 12 - Validation of thermal resistance results




a) PBGA 256 design with thermal vias

b) QFP PCDPH

Figure 13 - Relational complexity of auto-generated FEA models




*2D partial views of idealized 3D models*

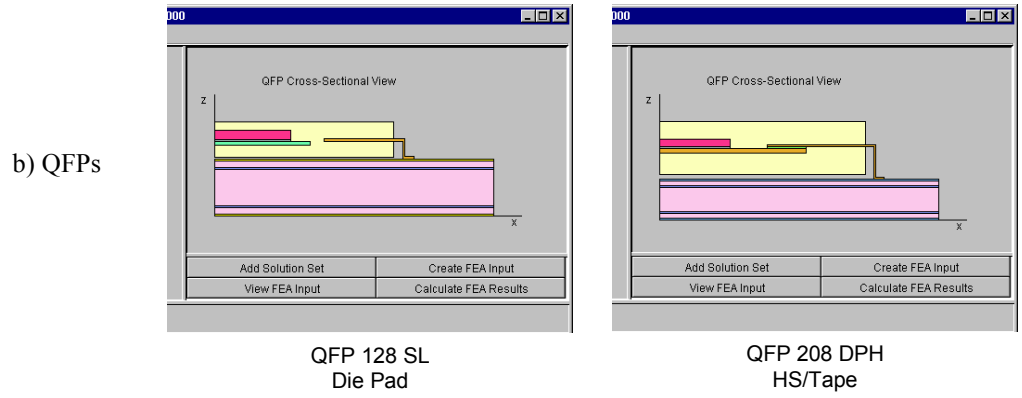



Figure 14 - Design variations with large impact on FEA mesh model

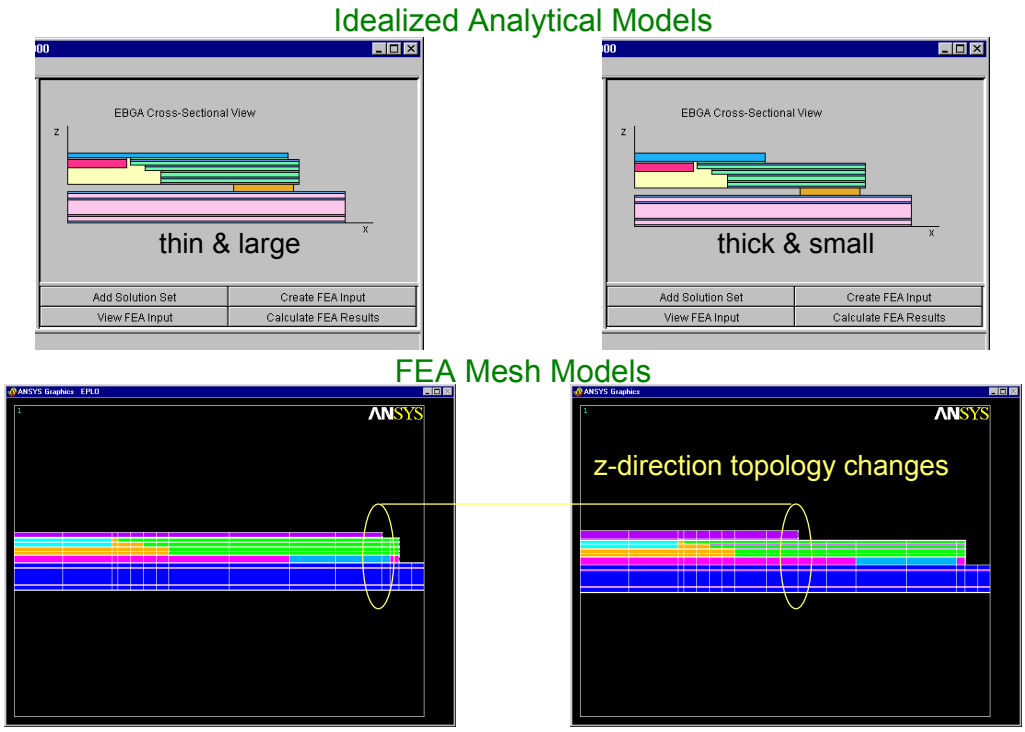



Figure 15 - Design change with moderate impact on FEA mesh model (heat spreader size variations in an EBGA 600 design)

Because of the reusable modular nature of the MRA, the same product model information that drives the above thermal analysis can be leveraged to also drive stress analysis. Figure 16 gives a basic stress analysis module tool interface (similar to Figure 8 for thermal analysis) and shows some of the auto-created FEA models. Note that different idealized geometry is present vs. the thermal analysis (e.g., distinct individual solder balls vs. smeared effective regions, as corner solder balls are typically where stress issues are greatest).

## 5. DISCUSSION

As implemented in Phase 1, these analysis models are hybrids of Category II and Category III problems (see Footnote 2) in that design geometry at the preliminary level is first created and then automatically transformed into an FEA model (a quasi-Category II situation). The user then manually improves that preliminary design geometry if necessary based on the previous analysis results, and then re-runs the analysis (again in an automated manner driven by the new preliminary design geometry). Once the preliminary design yields satisfactory analysis results (i.e., it is a CAE-approved design), it is used as the starting point for detailed package design (a quasi-Category III situation). Ideally the detailed package design would be checked by analysis periodically to ensure it stays on track as it evolves. Peak identifies how COBs support these types of multi-directional flows between CAD and CAE (Peak 2001).

The above results show that the VTMB methodology by Koo (2000) can produce algorithms that transform design-oriented product models into finite element models for automated solution. The analysis model creation burden is thus

Table 1 - Comparison of FEA Modeling Times (Koo 2000)

| *Analysis Model Creation Activity* | *With Traditional Practice* | *With VTMB Methodology*[4] | *Example* |
|---|---|---|---|
| Create initial FEA model (QFP cases) | 8-12 hours | 10-20 minutes | QFP 208 |
| Create initial FEA model (EBGA cases) | 6-8 hours | 10-20 minutes | EBGA 352 |
| Create initial FEA model (PBGA cases) | 8-10 hours | 10-20 minutes | PBGA 256 |
| Create variant–small topology change | 0.3-6 hours | (10-20)- minutes | Moderate dimension change (e.g., EBGA 600 heat sink size variations) |
| Create variant–moderate topology change | (6-8)- hours | (10-20)- minutes | Add more features (e.g., increase number of EBGA steps) |
| Create variant–large topology change | (6-8)+ hours | (10-20)- minutes or N/A | Add new types of features (e.g., add steps to EBGA outer edges) |

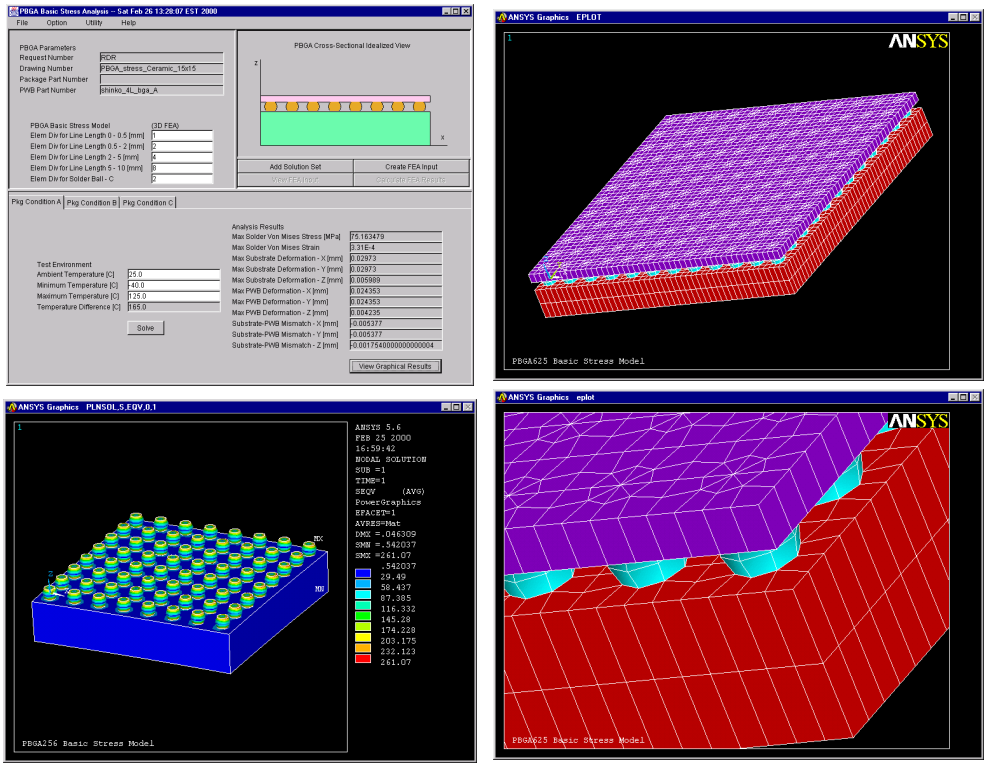



Figure 16 - Basic stress analysis module tool (via same product model as thermal analysis)

significantly reduced for the analysts, enabling them to focus on other more interesting problems.

A finite number of topological variation types can be supported in each algorithm, including changing numbers of layers, inclusion or omission of features, and re-sizing features that affect other bodies in the FEA model. However, supporting new classes of variations typically requires algorithm adjustment and subsequent re-coding and testing.

Work is underway to create algorithms that can handle broader classes of problems. The goal is to support analysis of new package types without having to re-code algorithms. Product model representations like STEP AP210 (AP210 2001) are under investigation in Phase 2 as a richer starting point to support such capabilities. Other enhancements envisioned include web application servers for full web-based operation (via thin clients) and information repositories to support collaborative design and analysis.

## 6. CONCLUDING REMARKS

This paper overviews a Phase 1 collaborative effort between Shinko and Georgia Tech to enable enhanced CAD-CAE interoperability. Analysis integration techniques based on engineering information technology have been applied to transform packaging expertise into highly automated analysis modules. Modules for various chip package families have been created to automate thermal resistance analysis and basic stress analysis - all driven from rich object-oriented product models.

Phase 1 work has achieved these benefits:

1) *Decreases FEA model creation time* (factor of 10:1 or more, from days/hours to minutes)

2) *Decreases total simulation process time* (75% in initial usage), which contributes to *reduced total customer response time*.

3) *Enables more analysis iterations* to study design variations, leading to an improved design.

4) *Enables analysis of more designs*, leading to enhanced customer interaction (e.g., providing them FEA graphics for all designs) and improved designs (e.g., verifying *all* designs via simulation vs. only doing apparent borderline cases).

5) *Provides new usage possibilities* via a web-based distributed architecture (e.g., increases potential user audience such as sales engineers around the world for quick customer feedback). This also can increase solution tool usage efficiency (more usage per license). It is one component in an enhanced collaborative product realization environment.

Other accomplishments include the following:

1) Introduced a methodology for formalizing and capturing analysis expertise (e.g., idealizations and modeling methods). This can be applied to other product families and other types of analysis.
   a) Enables greater automation and consistency.
   b) Captures trusted, customizable analysis procedures that yield reliable results.

2) Created a tool architecture towards generalized analysis integration (for other types of analysis).

3) Developed techniques for advanced product family automeshing (i.e., for variable topology multi-body (VTMB) FEA problems).

## ACKNOWLEDGMENTS

We are particularly grateful for the support of the following people: Yukiharu Takeuchi, Kuniyuki Tanaka, and Shin-ichi Wakabayashi of Shinko Electric Ltd.; Greg Bettencourt of Shinko Electric America, Inc.; and Bob Fulton and Chien Hsiung of Georgia Tech.

## REFERENCES[5]

AP210 (2001). Product Data Representation and Exchange: Electronic Assembly, Interconnect, and Packaging Design. ISO/IEC 10303-210. *http://www.ap210.com/*

Gordon, S. (2001). An Analyst's View: STEP-enabled CAD - CAE Integration. NASA STEP for Aerospace Workshop. *.http://step.jpl.nasa.gov/*

Koo, D. (2000). A Product Data-Driven Methodology for Automating Variable Topology Multi-Body Finite Element Analysis. Masters Thesis, Mechanical Engineering. Atlanta, Georgia Institute of Technology.

Peak, R. S. (1999). Integrating Product Design and Analysis Models. An Overview of ProAM: Product Data-Driven Analysis in a Missile Supply Chain. San Diego, CA, Assoc. for Enterprise Integration (AFEI)**:** Track 7, Session 3.

Peak, R. S. (2001). X-Analysis Integration / Multi-Representation Architecture (XAI/MRA) Overviews. *http://eislab.gatech.edu/*

Peak, R. S., R. E. Fulton, et al. (1998). "Integrating Engineering Design and Analysis Using a Multi-Representation Approach." Engineering with Computers **Vol. 14, No. 2.**: 93-114.

Peak, R. S., A. J. Scholand, et al. (1999). Product Data-Driven Analysis in a Missile Supply Chain (ProAM) Final Report, Concurrent Technologies Corp Contract N00140-96-D-1818/0008 for US DoD JECPO.

Peak, R. S., A. J. Scholand, et al. (1999). "Towards the Routinization of Engineering Analysis to Support Product Design." Intl. J. Computer Applications in Technology **Vol. 12, No. 1** (Invited Paper for Special Issue: Advanced Product Data Management Supporting Product Life-Cycle Activities) 1-15.

Wilson, M. (2000). Constrained Object Representation for Engineering Analysis. Masters Thesis, Mechanical Engineering. Atlanta, Georgia Institute of Technology.

XFW (2001). *XaiTools FrameWork*™ *http://eislab.gatech.edu/tools/XaiTools/*

[5] Some of these references are available at *http://eislab.gatech.edu/*